New Mesytec 32-channel VME ADCs: a status report

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In an effort to upgrade the electronics for detector readout and digitization we have purchased five 32-channel VME ADCs model MADC-32 from Mesytec [1]. Their specifications show that they have many desirable features such as: readout as one 32-channel ADC or two 16-channel ADCs (with separate gates), multiple voltage input modes (4V, 8V or 10V pulse ranges), multiple resolution settings (2k, 4k, or 8k channels), fast analog to digital conversion times (800 ns in 2k mode, 1.6 μs in 4k mode, and 6.4 μs in 8k mode), and especially lower power consumption when compared with other VME ADCs. The ADCs arrived in August 2008 from Mesytec, and we have tested and later used them in several experiments. Until now, these MADCs have been used to digitize signals from silicon detectors in exotic beam production tests with MARS, and in recent β-delayed proton-decay experiments. They will also be employed for experimental setups where large numbers of channels are needed, such as for the TECSA array.

The ADCs we have purchased were among the first to be produced after the prototype was released, and had a few problems. In the early tests, we found that when they were used with a CAEN 16-channel shaper model 568B, and connected by ribbon cables, they returned data "overflows" (= data in channel 3750 or above with "overflow" bit in data stream = 1) in channels that did not have signal in them. For example, a pulser signal in one channel, shaped by the CAEN shaper and then connected to the ADC via ribbon cable returned the correct data in the channel connected to the pulser, but would also return as many as 8 other channels with "overflow" readings. Similar results were observed when a Mesytec model MSCF-16 shaper was used in place of the CAEN shaper. These "overflows" were undesirable because not only they generated additional deadtime in the data acquisition system, but they also made analysis of the resulting data more difficult for cases where hit multiplicity was important.

To overcome this "overflow" problem, Mesytec has made changes in the hardware and upgraded the firmware in a few iterations. Four of these upgraded MADC-32 modules were replaced in May 2009 and have recently been tested under similar conditions to those above. With this upgraded hardware (V121-4508E and later) and new firmware (v1.26 and later) the ADCs function normally with ribbon cables and both the CAEN N568B and Mesytec MSCF-16 shapers, without presenting the "overflow" problem.

We have also tested the MADC-32 for resolution and linearity. We chose to conduct the tests using a germanium detector with a well-known linear electronics chain behind and a ^{152}Eu gamma-ray source. During the tests, we observed that even though the M-ADC is a "peak-sensing" ADC, in order to obtain good resolution, the "peak" of the shaped signal needed to be within 2 μs of when the signal gate opened. An example of a "good" versus a "bad" resolution spectrum for a ^{152}Eu source is shown in Fig. 1. As is clearly seen in the figure, if the peak of the signal was placed >2 μs after the signal gate is opened (top panel), the resolution was poor and the peaks in spectrum became asymmetric. Good resolution was restored simply by placing the peak of the signal earlier in the gate (bottom panel). Further tests with the M-ADCs revealed that this problem arose because of "the internal gate generator" feature of the ADCs
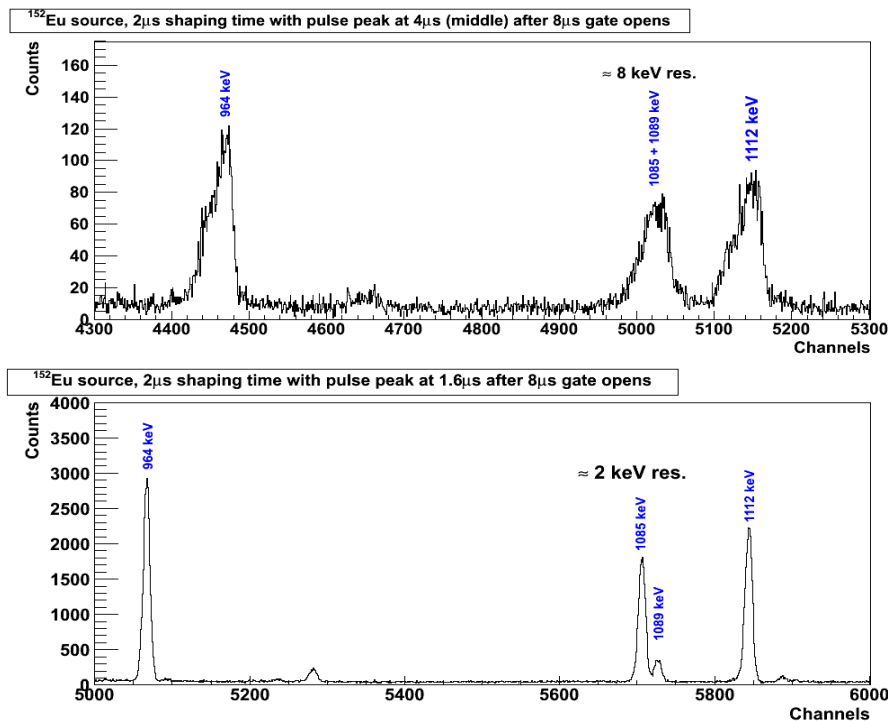
FIG. 1. Comparison of M-ADC generated spectra for different signal positions in the gate. When the M-ADC internal gate generator is used and gate width is not set up properly (see text for explanation).
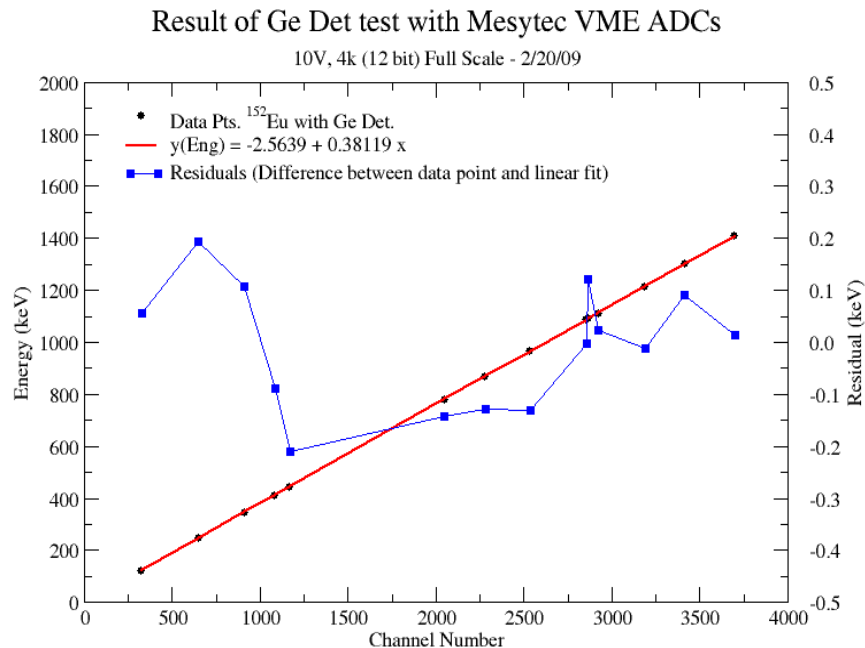

FIG. 2. Energy vs. channel (left scale) and the residues after linear fit (right scale) from the MADC-32 linearity test with a [152]Eu source and a germanium detector. The 10V input, 4k hi-resolution mode was used in this test. Overall, the non-linearity was observed to be < 0.1% for this test.

was enabled by default in the software and was not set up correctly. As a result, when the "peak" of the electronics signal came later in the signal gate as in the top panel of Fig. 1, the "peak" of the signal was actually outside the signal gate observed by the M-ADC internal gate generator. Thus, the good peak resolution of the bottom panel in Fig. 1 is restored by a) disabling the internal gate generator (now the default software setting or b) giving the internal gate generator a gate of proper width as described in the M-ADC manual. Note that if the internal gate generator is used one still must send the M-ADC a trigger pulse to start the gate generator.

The specifications of the M-ADC claim that the differential non-linearity (DNL) is < 1% over the entire range of channels regardless of the voltage input or resolution mode used [1]. The worst non-linearity observed during the test was 0.4% in the 10 V input, 8k low-resolution mode, while typical non-linearity over the entire range of data channels was observed to be < 0.1%. The results of the linearity tests of the M-ADCs for in 10V input, 4k high-resolution mode with the Germanium detector and the ^{152}Eu source are shown in Fig. 2.

There were a few problems with the new M-ADCs related to hardware and firmware problems. These problems with phantom "overflows" in the data stream and spectrum resolution have been largely overcome. As a result of these tests, the M-ADCs are now available at the Cyclotron Institute for use in future experiments.

[1] M-ADC manual: http://www.mesytec.com/datasheets/MADC-32.pdf